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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,125	02/18/2004	Christopher S. Johnson	400.149US02	3355

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,125	JOHNSON, CHRISTOPHER S.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-21,35-37 and 42-44* is/are allowed.

6)☒ Claim(s) *1,2,4,5,8,22,26-28,30,34 and 38* is/are rejected.

7)☒ Claim(s) *3,6-7,23-25,29,31-33,39-41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 04/20/2006 has been entered.

2. Claims 1-44 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

After carefully reviewing the last applicant's arguments, examiner think that applicant must understand that examiner spend a lot of time to make your invention is a valid invention. With understanding of examiner, examiner tries to search in the best and sent the best cited arts to applicant. Examiner does not want to hold application but examiner does not want to issue an invalid invention. Otherwise, applicant can file a notice of appeal. To avoid a confusing, examiner required next reply of applicant should be used exactly the limitation used in claim. Because examiner searched word by word, the limitation is appeared in the claim. For example, " to configure" is limitation in claim invention. In last reply filed on 04/20/2006, applicant uses **"reconfiguration"** to against to reference, the reference does not including any reconfiguration. It is improper, because the 'reconfiguration' is different from "configuration", which is not appearing in claim.

Claim Objections

4. Because the number of X, Y and Z do not specified. Examiner doe not what state is used, which is one of first state and second state of mode register when Y=Z.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2,4-5,8,22,26-28,30,34,38 are rejected under 35 U.S.C. 102(b) as being anticipated by Kellogg et al. (U.S. Patent No. 5,896,404).

Regarding claim 1, Kellogg et al. disclose a system (Figure 2), comprising:

a controller (Column 1, lines 20-30, *processor, processor provides clock.. controller is processor*); and

a memory device (Figure 2, 140) coupled to the controller to receive signals therefrom (Figure 2, memory device 140 receives signals RXCLK, COMMAND from processor controller) , and comprising:

an array of memory cells (Figure 2, array of memory cells includes banks 142, 144,146,148) arranged in a plurality of addressable banks (Figure 2, banks 142-148) , each bank comprises addressable rows and columns of memory cells (Column 2, lines 20-23, DRAM array is divided into two or more banks, with sub-array cells arranges in addressable rows and columns) ;

a mode register (Figure 2, mode register including 150, 154,156,158,160, Figure 3, 170, mode register is mode select in Figure 2 or 170 in Figure 3, Column 3, lines 61-62 is defined setting a bit in a mode register); and

address circuitry (Figure 3, 128, Figure 3, 168, address into address circuitry 128, Column 3, lines 2-3, an address may received from I/O circuitry 126) coupled to the mode register (Figure 2, mode register coupled address circuitry 128) to configure the addressable banks (Column 3, lines 37-39, In ECC mode , page registers 154-160 are reconfigured) in response to a program state of the mode register (Column 3, lines 37-39,).

(Figure 2, address circuitry 128 coupled to the mode register (150, 154, 156, 159, 160) to the addressable banks 142,144,146,148 in response to program state ECC of mode register 150 by to transfer seventy-two-bits of data to/from seventy-two bit bus 118 from memory banks 102-108, column 3, lines 37-39. As described above, examiner believes Kellogg et al. clearly disclosed each limitation in claim 1 of present applicant). (**configuration and *reconfiguration*** *this limitation is defined in last remark in page 11, line 3*).

Regarding claim 2, Kellogg et al. disclose wherein the addressable banks can be configures as either four or eight banks (Figure 2, addressable banks configured into 4 banks 142,144,146,148 or more banks in column 2, lines 21, or unlimited as defined in column 3, lines 12-20).

Regarding claim 4, Kellogg et al. disclose a system (Figure 2), comprising:

a controller (Column 1, lines 20-30, *processor, processor provides clock.. controller is processor*); and

a dynamic random access memory device (ABSTRACT, Figure 2, 140) coupled to the controller to receive signals therefrom (Figure 2, memory device 140 receives signals RXCLK, COMMAND from processor controller) , and comprising:

an array of memory cells (Figure 2, array of memory cells includes banks 142, 144,146,148) arranged in a plurality of addressable banks (Figure 2, banks 142-148) , each bank comprises addressable rows and columns of memory cells (Column 2, lines 20-23, DRAM array is divided into two or more banks, with sub-array cells arranges in addressable rows and columns) ;

an array of X memory cells (Figure 2, 142-148 with 64x256x1024 memory cells).

a mode register (Figure 2, mode register including 150, 154,156,158,160, Figure 3, 170, mode register is mode select in Figure 2 or 170 in Figure 3, Column 3, lines 61-62 is defined setting a bit in a mode register); and

address circuitry (Figure 3, 128, Figure 3, 168, address into address circuitry 128, Column 3, lines 2-3, an address may received from I/O circuitry 126) coupled to the mode register (Figure 2, mode register coupled address circuitry 128) to configure the addressable banks (Column 3, lines 37-39, In ECC mode , page registers 154-160 are reconfigured) in response to a program state of the mode register (Column 3, lines 37-39), wherein the mode register defined a number of addressable banks of the array (Column 3, lines 28-45, Kellogg et al. disclosed a number of addressable banks of the array memory cell is defined by in Normal mode or ECC mode, in Normal mode is sixty-four bits, in ECC mode is seventy-tow bit).

Regarding claim 5, Kellogg et al. disclose wherein a first state of the mode register configures the array into Y banks each having X/Y memory cells, and a second state of the mode register configures the array into Z banks each having X/Z memory cells (Column 3, lines 12-23, Kellogg et al. disclosed a first state is Normal mode, a second state is a ECC mode, and banks of memory depending from each mode).

Regarding claim 8, Kellogg et al. disclose wherein the address circuitry comprises a multiplex circuit (Figure 2, 128 is a MUX, column 4, line 43).

Regarding claims 22, 27, 30, Kellogg et al. disclose a system (Figure 2) comprising:

a controller providing an input signal (Column 1, lines 38-46, processor) ; and

a dynamic random access memory device (Figure 2, 140) coupled to the controller and comprising an array of X memory cells (Figure2, 142-148) ; a decode circuit (Figure 3, 178) to decode circuit to configure the array in response to a program state of the input signal (Figure 3, 172, Column 3, lines 60-65, input 172), and address circuitry coupled to the decode circuit to configure the array (Column 3, lines 37-39) in response to a program state of the input signal (Column 3, lines 37-45, program state is ECC mode or Normal mode) , wherein the input signal defines a number of addressable banks of the array(Column 65-67, Column 4, lines 1-32).

Regarding claims 26, 34, Kellogg et al. disclose wherein the address circuitry comprises a multiplex circuitry (Figure 2, 128).

Regarding claim 28, Kellogg et al. disclose wherein the addressable banks (ABSTRACT, addressable banks, which includes address rows and columns as defined in claim 1) can be configured as either four or eight banks (Figure 2, 4 banks).

Regarding claim 38, Kellogg et al. disclose a method of operating a memory device (Column 3, lines 60-63) comprising:

receiving an external input signal at decode circuitry of the memory device (Figure 2, 172) ; and adjusting address circuitry of the memory device (figure 2,128) in response to the decoded external input signal, wherein the address circuitry configures a number of address banks of a memory cell array (Figure2, Column 3, lines 28-53, Figure 3, Column 54-65).

Allowable Subject Matter

7. Claims 3, 6-7, 23-25,29,31-33,39-41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 6-7, 23-25,29,31-33,39-41 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kellogg et al. (U.S. Patent No. 5,896,404), and others, does not teach the claimed invention having an address circuitry selectively routes address signals to either a row decoder or a bank decoder in response to the mode register as claims 3, 6-7, 23-25,29,31-33,39-41 disclosed.

8. Claims 9-21,35-37, 42-44 are allowed.

Claims 9-21,35-37,42-44 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kellogg et al. (U.S. Patent No. 5,896,404), and others, does not teach the claimed invention having address signal circuitry coupled to a plurality of address signal input connections, the address signal circuitry routes a selected one of the plurality of address input connections to either the row or bank address decoder in response to data stored in the mode register.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

7/03/2006